Course Code	Course Title	С	Н	Ι	Ε	Т
17U2DMC4	COMPUTER ORGANIZATION AND ARCHITECTURE	4	5	25	75	100

UNIT I: Basic Computer Organization

Instruction Codes – Computer Registers – Computer Instructions – Timing and Control – Instruction Cycle – Control Memory – Address Sequencing.

UNIT II: CPU

General Register Organization – Stack Organization – Instruction Formats – Addressing Modes – Program control.

UNIT III: Computer Arithmetic

Hardware Implementation and Algorithm for Addition, Subtraction, Multiplication, Division – Booth Multiplication Algorithm – Floating Point Arithmetic.

UNIT IV: I/O and Memory Organization

I/O Interface – Asynchronous Data Transfer – Modes of I/O Transfer – Priority Interrupt – Direct Memory Access - Memory Hierarchy – Main Memory – Auxiliary Memory – Associative Memory – Cache Memory – Virtual Memory.

UNIT V : Advanced Processing

RISC, CISC Characteristics - Parallel Processing – Pipe Lining – vector processing – array processors – Multi processors – Interconnections structures.

Text Book:

M. Morris Mano, Computer System Architecture, Third Edition, 2003, Prentice Hall of India.

Chapters:

Unit I: 5.1 to 5.5, 7.1 to 7.2, Unit II: 8.1 to 8.5, 8.7, Unit III: 10.1 to 10.5 Unit IV: 11.2 to 11.6, 12.1 to 12.6 & Unit V: 8.8, 9.1, 9.2, 9.6, 9.7, 13.1, 13.2

Reference Books:

A. S. Tanenbaum, Structured Computer Organization, PHI.
M.Morris Mano , Digital Logic & Computer Design, 2006, PHI.
Alan B.Marcovitz, Introduction to Logic design, 2nd edition, 2005, TMH.

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Page 269